WHAT IS CLAIMED IS:

1. A method of forming a spacer, comprising the steps:

depositing a spacer layer over a substrate and a gate electrode having a top surface and vertically extending sidewalls;

forming a protective layer on the spacer layer;

etching the protective layer to remove the protective layer from the spacer layer over the top surface of the gate electrode and maintain the protective layer on the spacer layer parallel to the sidewalls of the gate electrode;

etching the spacer layer to remove the spacer layer from the substrate and over the top surface of the gate electrode to form spacers on the gate electrode with each spacer having two substantially vertical sidewalls extending parallel to the gate electrode sidewalls.

2. The method of claim 1, wherein the spacer layer is deposited to a thickness greater than 200 Å.

3. The method of claim 2, wherein the protective layer is formed to a thickness between about 10 Å to about 100 Å.

4. The method of claim 3, wherein the spacer layer is a nitride and the protective layer is an oxide.

5. A method of forming a semiconductor device, comprising the steps:

forming a gate electrode having vertically extending sidewalls on a substrate;

forming first sidewall spacers on the gate electrode, each first sidewall spacer having a pair of vertically extending planar sidewalls that are substantially parallel to the gate electrode sidewalls; and

performing a source/drain implantation with the gate electrode and the first sidewall spacers masking the substrate.

6. The method of claim 5, wherein the step of forming first sidewall spacers includes:

depositing a spacer layer over the substrate and the gate electrode;

forming a protective layer on the spacer layer; and

etching the protective layer and the spacer layer to form the first sidewall spacer.

7. The method of claim 6, wherein the step of etching includes dry etching the protective layer to remove the protective layer except for vertically extending portions of the protective layer that are planar and substantially parallel to the gate electrode sidewalls.

8. The method of claim 7, wherein the step of etching further includes etching the spacer layer to remove the spacer layer from the substrate and over a top surface of the gate electrode, leaving the spacer layer between the gate electrode sidewalls and the vertically extending portions of the protective layer.

9. The method of claim 8, further comprising forming a second sidewall spacer in the first sidewall spacer.

10. The method of claim 8, wherein the spacer layer is etched with an etchant that is highly selective to the spacer layer and does not substantially etch the protective layer.

11. The method of claim 10, wherein the spacer layer is deposited to a thickness of between about 200 Å to about 1000 Å.

12. The method of claim 11, wherein the protective layer is deposited to a thickness of between about 10 Å to about 100 Å.

13. A semiconductor device comprising:

a substrate;

a gate on the substrate, the gate having vertical sidewalls; and

sidewall spacers on the gate sidewalls, the sidewall spacers having a rectangular cross-section and extending vertically to greater than half the height of the gate; and

ion implanted source/drain regions defined by the sidewall spacers.